IMP-2
Hardware User Manual

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Chapter 1 Overview

1.1. Introduction

The Intelligent Motion control Platform, IMP-2, employs the Intelligent Motion control Chip (IMC) developed by the MSL of ITRI and is capable of evenly sending the pulse translation for each axis through the Pulse Generator Engine (PGE) (Note 1) based on the Digital Differential Analyzer (DDA) principle to realize the 8-axis synchronous/asynchronous motion control. During the pulse output control period, it allows the encoder to read the motor's encoding values from its input terminal so it is suitable for pulse command servo motor or stepper motor control.

The IMP-2 hardware closed loop control uses the PID and FF (FeedForward, Note 2) control algorithm to provide output voltage between -10V and 10V for driving speed command servo motors. It can be used for multi-axis high-precision servo control. Each axis has a set of input that includes mechanical home position, forward limit point, and backward limit point. In addition, it also provides Servo On outputs, Position Ready outputs, and Emergency Stop inputs.

The IMP-2 has a built-in microprocessor (Power PC440) with hardware Double Precision Floating Point Unit. By running the Real-Time Operating System (RTOS), it can be used to construct an embedded motion control platform which can be operated in the Standalone mode to carry out the motion control mission. Besides, standalone motion control operations integrated with the general PCI-Bus and Ethernet Controller to communicate with external devices. The user can use a personal computer or other user interface to operate the IMP-2 through the network for sending motion commands and monitoring remotely. In addition, it is also integrated with the General Servo Bus (GSB) to communicate with full digital servo drive with its own communication module, and connecting various dedicated communication module boards.

The expansion I/O can be used to connect the Asynchronous Remote Input/Output board (IMP-ARIO) which allows for the expansion up to 512 inputs and 512 outputs.

Note 1: For the PGE, please refer to Fig. 1-8 and Fig. 1-9.
Note 2: For the PID and FF control algorithm, please refer to Fig. 1-7.

1.2. IMP-2 Hardware Specifications

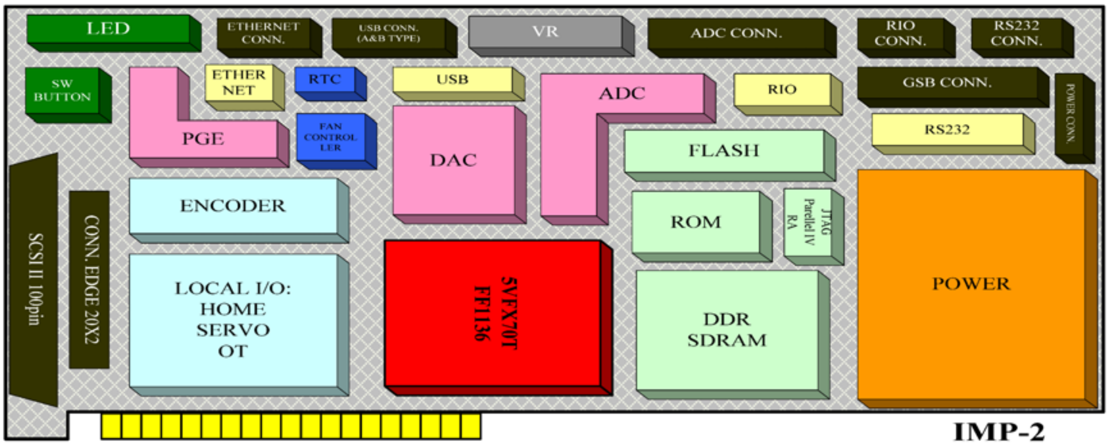


Fig. 1-1

Motion		Peripheral	
PGE	32-bit	CPU	32-bit RISC 400MHz
ADC Interface	14-bit x 8 Channels	PCI-Bus	32-bit
DAC Interface	16-bit x 8 Channels	GSB (General Servo Bus)	SSCNET III MECHATROLINK III
Encoder Interface	32-bit x 8 Channels	Flash	32MB
Position Control Loop	8 Axes (PID & FeedForward Control)	PROM	32MB
LIO (on board)	42 Input/Output	RS232	1 Set
RIO	512 Input/512 Output	USB	1 Set (USB2.0)
Timer	32-bit	DDR	128MB
Watchdog timer	32-bit	Ethernet	1 Set (10/100Mbps)

Note:

PGE: Pulse Generator
ADC: Analog to Digital Converter
DAC: Digital to Analog Converter
LIO: Local Input/Output
RIO: Remote Input/Output
GSB: General Servo Bus

1.3. Connection Diagram and Description

The IMP-2 can be operated in A^+ PC mode and standalone mode, which are described as follows:

The A^+PC mode allows the user to develop, compile, and execute application software using a personal computer. All the motion control functions in the application software can communicate with the IMP-2 through the A^+ PCI Mode (Tight link) or A^+ Ethernet Mode (Loose link), and the related motion control functions are computed and processed by the IMP-2; the user interface and other application functions are computed and processed by the personal computer.

Refer to Fig. 1-2 and Fig. 1-3: The A^+ PC mode allows the user to use the PCI-Bus or the Ethernet to connect the IMP-2 and send motion control commands via the PC.

Refer to Fig. 1-4: In the standalone mode, the user should upload the program to the IMP-2. In this case, when the IMP-2 is connected with an external power, it can execute the motion control commands. In this mode, even though it is not connected with a PC, the user can still use various types of user interface to monitor the trajectory planning operation.

Refer to Fig.1-2~Fig.1-4: In the A^+ PC mode and standalone mode, the IMP-2 can send motion control commands to the drives and motors through the SCSI II 100-Pin and SCSI II 68-Pin connection cable with the IMP-WB-1/2. The IMP-WB-1/2 provides wiring terminals for connecting the Local I/O for the user. Furthermore, the IMP-2 provides remote I/O interface which can connect up to 32 sets of IMP-ARIO for controlling the Remote I/O.

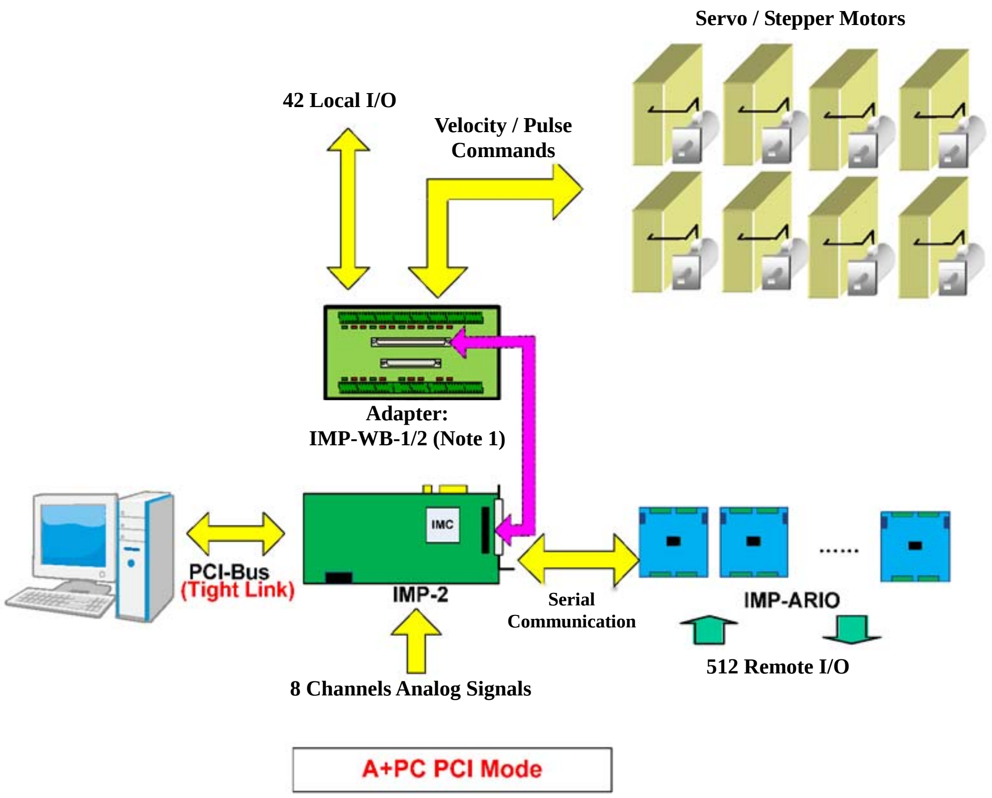


Fig. 1-2

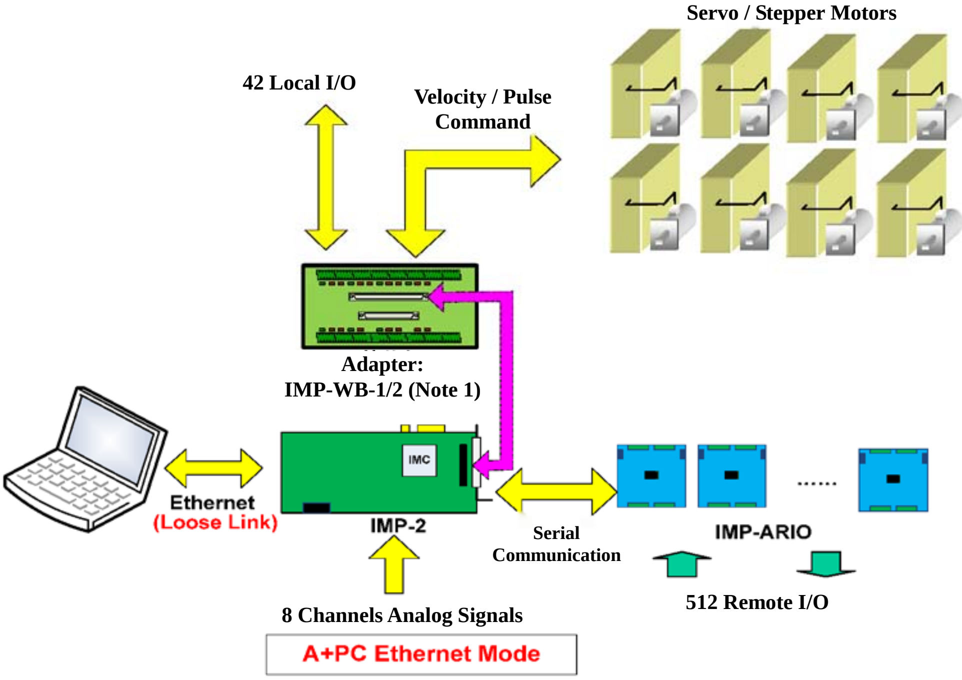


Fig. 1-3

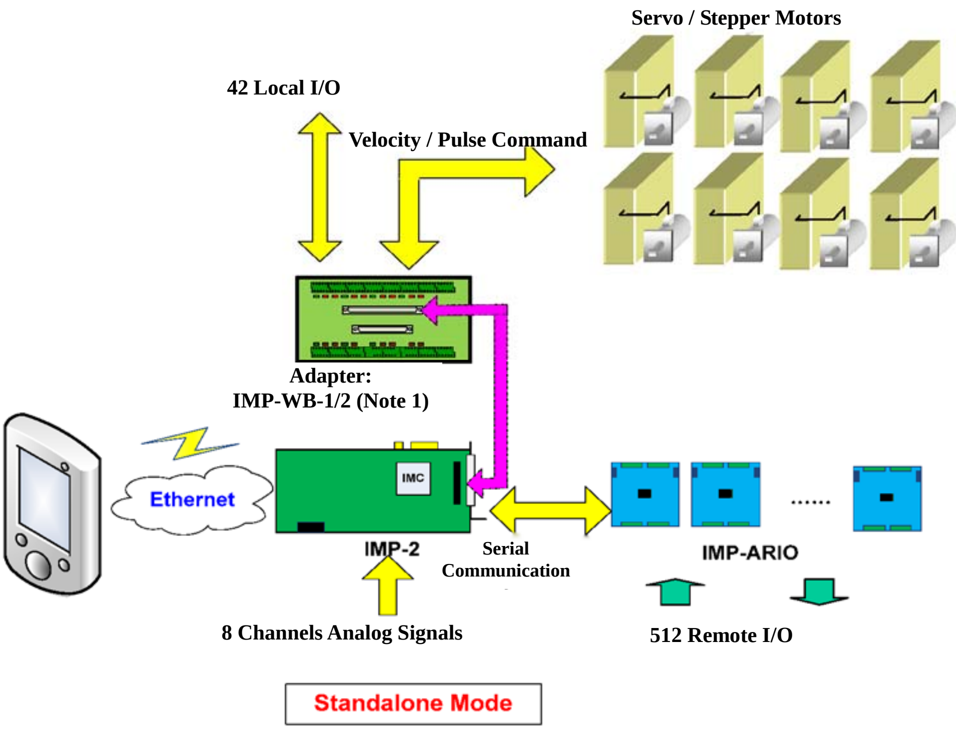


Fig.1-4

Note 1: Available adapters.

IMP-WB-1: Universal adapter.

IMP-WB-2: Dedicated adapter for Panasonic (Panasonic Minas A5). This adapter is also workable with using specific adapter cable for specific manufacturers (Mitsubishi MR-J3, Delta ASDA-A2, Yaskawa Σ-V)

1.4. Software Support

The IMP-2 software includes a real-time multi-tasking operation system (VxWorks), a trajectory interpolation calculation, integration and development kits, motion control library, and several development tools to provide the user a complete, from basic to advanced, system development process.

In the A^+ PC mode, the user can use Visual C++ / Basic / C# to develop the application software. While in the standalone mode, the user can use the WindRiver Workbench 3.2 to develop the application software.

The IMP-2 provides the user various IDDL and MCCL functions as described below:

- IDDL (IMC Device Driver Library)---IMP Series Device Driver Library

It has more than 120 functions for the users to call. For more details, please refer to the "IMP Series Device Driver Library User Manual" and "IMP Series Device Driver Library Reference Manual".

- MCCL (Motion Control Command Library)---IMP Series Motion Control Command Library

It provides motion control function as 2D and 3D point-to-point, line, curve, circle, helix and other userful control commands, which allows the user to configure the mechanical and motion parameters. It provides approximately 250 functions in total. For more details, please refer to the "IMP Series Motion Control Command Library User Manual" and "IMP Series Motion Control Command Library Reference Manual".

1.5. Function Descriptions

Functional Block Diagram of the IMP-2

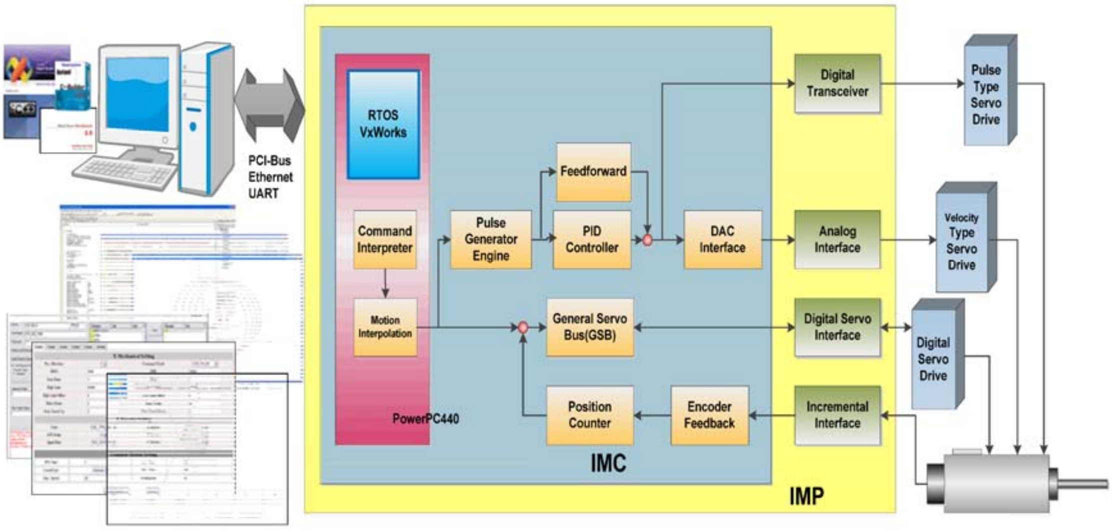


Fig. 1-5

The main functional block diagram is shown below. The IMP-2 provides 8-axis synchronous/asynchronous open loop control (pulse command), 8-axis synchronous /asynchronous closed loop control (velocity command), Local I/O, Remote I/O, A/D converters, D/A converters and etc., which are described in the following sections.

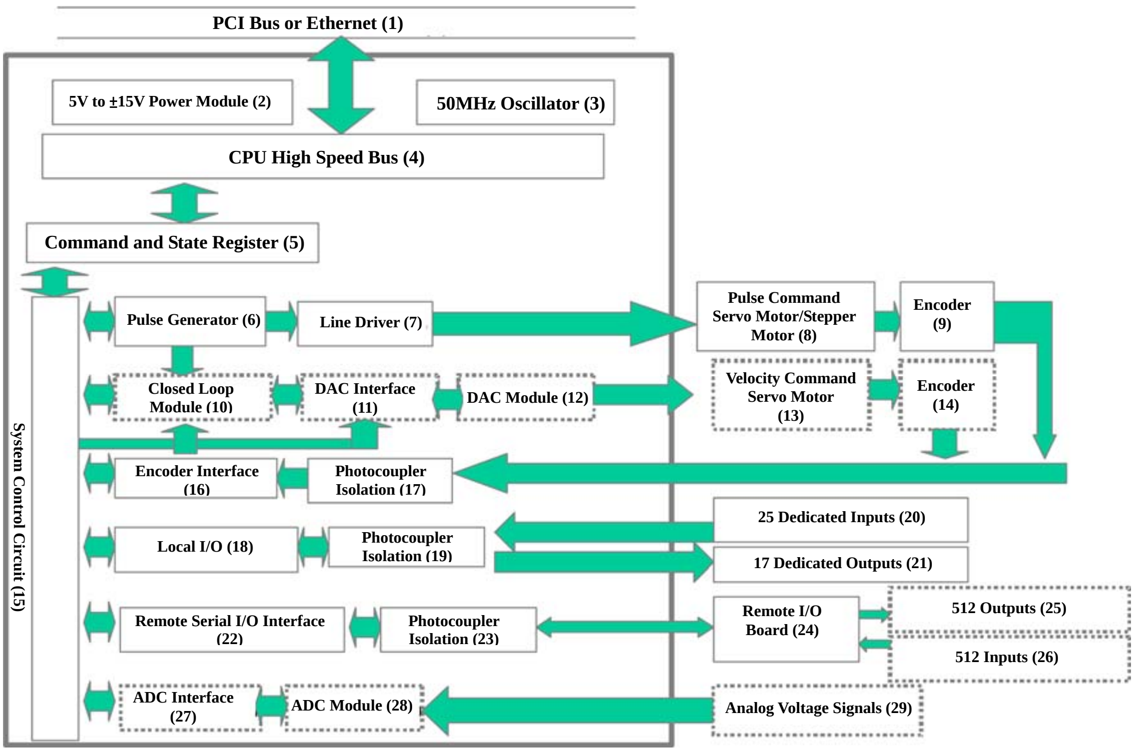


Fig. 1-6

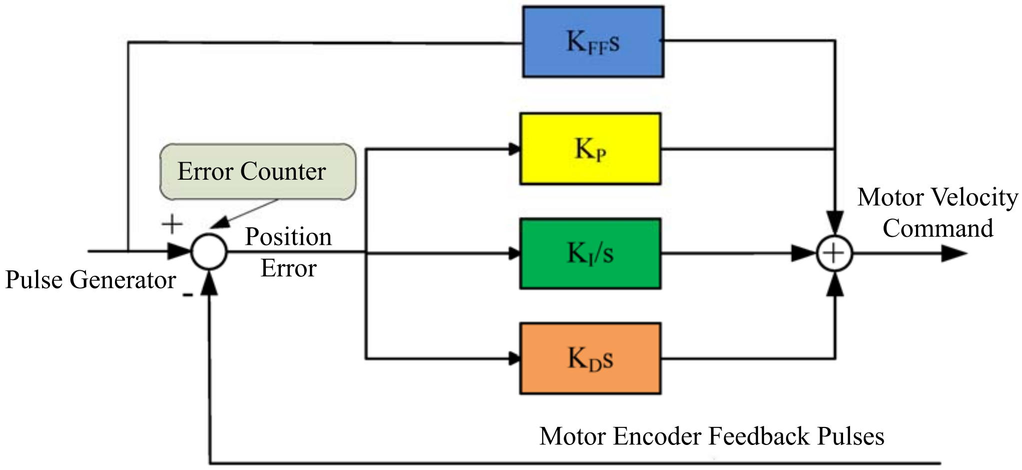
1.5.1. 8-Axis Synchronous/Asynchronous Open Loop Control (Pulse Command)

Refer to the functional block diagram of the IMP-2 (Fig.1-6): When the IMP-2 receives the motion control commands commenced by the user, the motion control commands will be transmitted through the ***PCI Bus*** or ***Ethernet (1)*** to the internal ***CPU High speed Bus (4)*** of the IMP-2 and then sent to the internal ***Command and State Register (5)*** and ***System Control Circuit (15).*** In the end, the commands drive the internal to evenly generate the pulses (Pulse Command) (Three formats selectable: A/B phase, CW/CCW, and Pulse/Direction). The pulses through the ***Line Driver (7)*** (MC3487) in differential signals to feed the external motor driver to drive the pluse mode of ***Servo Motor/Stepper Motor (8)***; The motor's ***Encoder (9)*** signal via the ***Potocoupler Isolation (17)*** into the ***Encoder Interface (16),*** and then the signal will be stored in the ***Command and State Register (5)*** through the ***System Control Circuit (15)***.

1.5.2. 8-Axis Synchronous/Asynchronous Closed Loop Control (Velocity Command)

Refer to the functional block diagram of the IMP-2 (Fig.1-6): When the IMP-2 receives the motion control commands commenced by the user, the motion control commands will be transmitted through the ***PCI Bus*** or ***Ethernet (1)*** to the internal ***CPU High speed Bus (4)*** of the IMP-2 and then sent to the internal ***Command and State Register (5)*** and ***System Control Circuit (15).*** In the end, the commands drive the internal ***Pulse Generator (6)*** to evenly generate the pulses (Pulse Command),which will be sent to the ***Closed Loop Module (10)*** while the feedback signal from the motor's ***Encoder (14)*** (differential signal) transmits back to the IMP-2. The signals are received and isolated by the ***Photocoupler (17)*** prior to entering the ***Encoder Interface (16)*** for signal processing (including filtering) and then fed into the ***Closed Loop Module (10)*** for calculation. The ***Closed Loop Module (10)*** carries out the feedback control based on the PID and FF algorithm (Note 1) according to the number of pulses from the Pulse Generator and the number of pulses feedback from the encoder. The resultant signal will drive the ***DAC Module (12)*** (including AD1866R and TL074 amplification stage) through the ***DAC Interface (11)*** (D/A ➔Digital to Analog) to generate a voltage signal between -10V and +10V (Velocity Command). In the end, the speed command is sent to the ***Velocity Interface Servo Motor (13)*** (Note 2) through the IMP-WB-1/2.

Note 1: The closed loop control of PID and FF control algorithm is described in Fig. 1-7.



- The Position Error (i.e., the Error Signal) will be recorded by the error counter. Position error = Pulse Generator – Feedback Pulses from the Motor Encoder.

Fig. 1-7

Note 2: The velocity mode of the servo motor: The motor driver uses the velocity command input format (the velocity command is expressed by a voltage signal). The typical range of the voltage input is from -10V to +10V, which corresponds to the maximum backward speed to the maximum forward speed of the motor's rotation. The speed is a linear response to the input voltage.

1.5.3. Overview of IMP's Motion Core Mechanism

(I) Open loop and Closed Loop Control Mechanism

1. The IMP-2 has 8 sets of motion control core mechanisms, where each can be configured as one of the following two Output Control Modes:
   ----Closed Loop Control (Velocity Command).
   ----Open Loop Control (Pulse Command).
   M sets of closed loop control and N set of open loop control are available for configuration by the user , where the criterion M+N≦8 must be satisfied.
2. The hardware resources corresponding to each control core on the IMP-2 are as follows:
   ----1 set of Closed Loop Control Core [Closed Loop Control Core = ***Pulse Generator (6)*** + ***Closed Loop Mechanism (10)***].
   ----1 set of Open Loop Control Core [Open Loop Control Core = ***Pulse Generator (6)*** + ***Line Driver (7)***].
   ----1 set of DAC = ***DAC Interface (11)*** + ***DAC Module (12)***.
   ----1 set of Encoder Interface = ***Encoder Interface (16)*** + ***Photocoupler Isolation (17)***.
3. When a certain Control Core is configured for Open Loop Control (Pulse Command), the IMP-2 will use the ***Pulse Generator (6)*** of the Control Core and a set of ***Line Driver (7)***. In this case, the associated DAC and Encoder Interface of the Control Core are available for separate operations. On the contrary, if it is configured for Closed loop Control (Velocity Command), the IMP-2 will use the ***Pulse Generator (6), Closed Loop Module (10)***, a set of DAC output, and a set of Encoder Interface of the Control Core. In this case the associated ***Line Driver (7)*** of the Control Core is not activated.
4. Example
   If the user configures the IMP-2 with 6 sets of Closed Loop and 2 sets of Open Loop Controls, the hardware resource allocations of the IMP-2 are as follows:
   ➔6 sets of Closed Loop Control: It requires 6 sets of Control Core, 6 sets of DAC, and 6 sets of Encoder Interface
   2 sets of Open Loop Control: It requires 2 sets of Control Cores and 2 sets of ***Line Driver (7)***.
   As a result,
   8 Control Cores ---- all in use.
   8 ***Line Drivers (7)*** ---- 2 line drivers are in use and the remaining 6 line drivers cannot be used (because 6 line drivers of Closed Loop Controls are used).
   8 DACs ---- 6 DACs are occupied and the remaining 2 DACs are available for separate operations.
   8 Encoder ---- 6 encoders are in use and the remaining 2 encoders are available for separate operations.

(II) For the principle of the Pulse Generator, please refer to Fig.1-8 and Fig.1-9 as below.

Function:

The user commences the Pulse Generator Positioning Command (i.e., the number of the encoder pulse to the driver motor) and the time required to execute the command (i.e., the Interpolation Time, IPO Time) after calculated, the Pulse Generator can generate the pulses with the corresponding number of the encoder pulse to evenly transmit it within the IPO Time.

Description 1:

Refer to the following figure. If the positioning command is for forward 1000 encoder pulse (assuming that the initial position of the motor is at the 0th pulse, and the interpolation time (IPO Time) of the command is 0.5 second), then the Pulse Generator is generate send 1000 pulses in 0.5 second which allows the motor to rotate (at a constant speed) 1000 pulses.

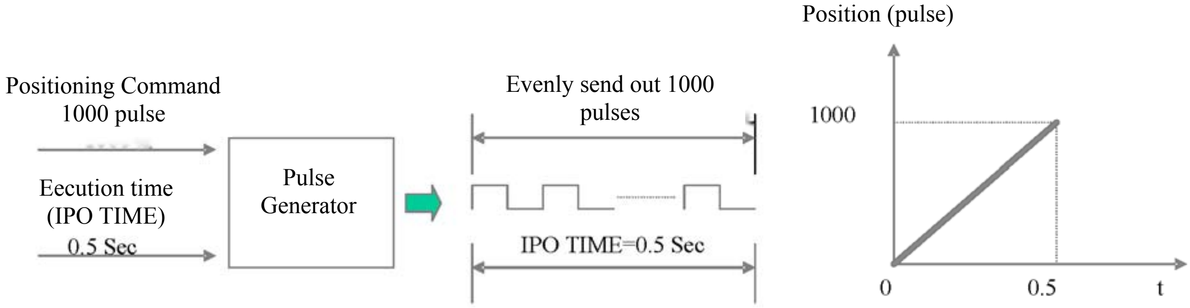


Fig. 1-8

Description 2:

Refer to the following figure. The horizonial axis indicates the time, in which △t represents the IPO Time. The vertical axis indicates the number of pulse by which the motor rotates.

Zone I: The motor rotates forward from the 0th pulse to 1000 th pulse at a constant speed in the positive direction.The rotation speed is 1000 pulse /△t

Zone Ⅱ: The motor stops at the position of 1000 th pulse.

Zone Ⅲ: The motor rotates forward from 1000 th pulse at a constant speed till it reaches 1500 th pulse. The rotation speed is 500 pulse /△t

Zone Ⅳ: The motor remains still at 1500 th pulse.

Zone Ⅴ: The motor rotates backward from 1500th pulse till it reaches 0th pulse. The rotation speed is 1500 pulse /△t. The more pulses within the same time interval △t, the faster it rotates and the farther it travels. For the same number of pulses, the smaller △t is, the faster the motor rotates.

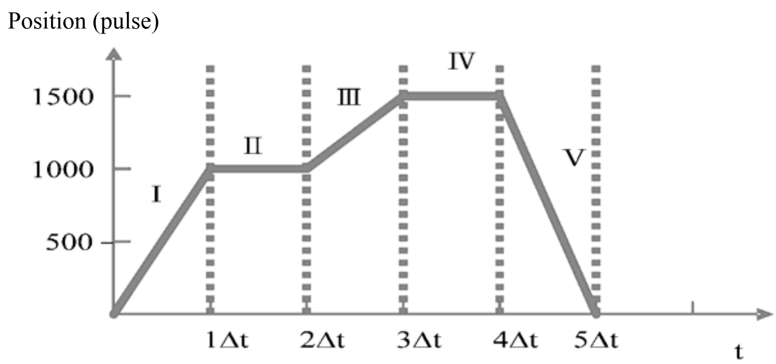


Fig. 1-9

(III) There are three formats of the pulse commands sent from the Pulse Generator: Pulse / Direction, CW/CCW, A/B phase. It should be configured according to the motor's acceptable format as shown in Fig. 1-10 below.

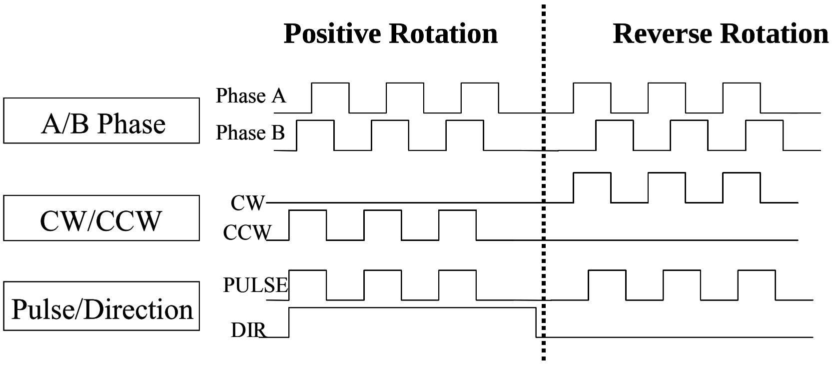
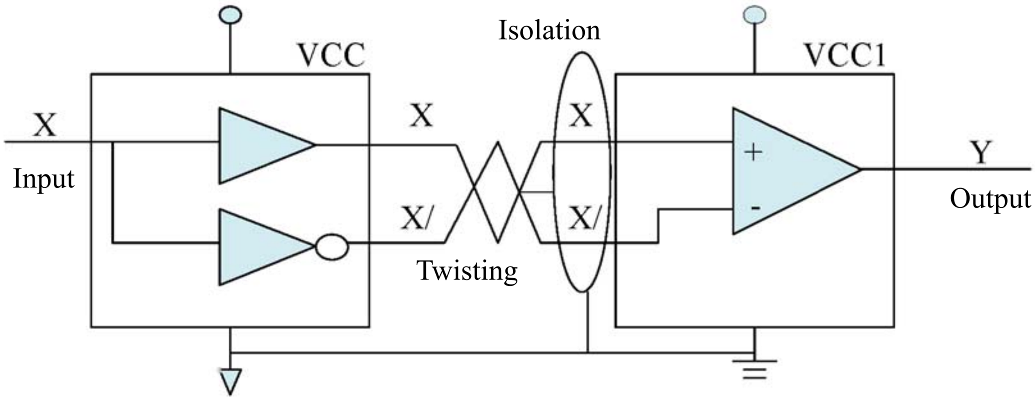


Fig. 1-10

(IV) The Differential Transmission is described in Fig. 1-11 as below.



Input	Signal in the Cable		Output
X	X	X/	Y
0	0	1	0
1	1	0	1

※ The sending side converts signal X into X and X/ output signals
※ The receiving side compares signals X and X/ and converts it into Y signal
※ The truth table is as shown in the left figure
※ The differential transmission can effectively eliminate the common mode noise.
※ The reference ground of the input terminal and the output terminal should be connected to prevent the input terminal and the output terminal from being damaged due to different electric potentials
※ It is recommended to transmit the signal using the twisted pair with shielding mesh

Fig. 1-11

(V) Pulse format transmitted from the IMP-2 as shown in Fig. 1-12 below.

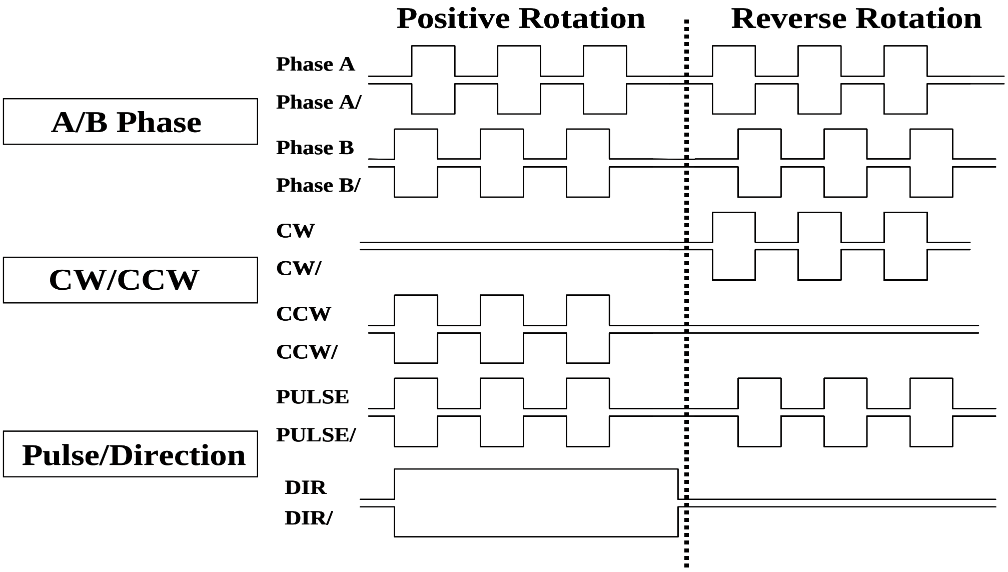


Fig. 1-12

(VI) The user can select the Encoder Interface to use the Index signal input with the formats of A/B phase, CW/CCW, or Pulse/Direction. When the A/B phase is selected, it allows the encoder input signal to be multiplied by 0x (input disabled), 1x, 2x, or 4x.

1.5.4. Local Digital Input/Output

Refer to the functional block diagram of the system as shown in Fig. 1-6: When the IMP-2 receives the motion control commands commenced by the user, the commands will be fed into the IMP-2 through the ***PCI-Bus*** or ***Ethernet (1)***. The IMP-2 will carry out the data reading or writing operation for the ***Local I/O (18)***. The output signals are via the ***Photocoupler Isolation (19)*** and then amplified to increase the driving capability to connect the external device. The input signals are also via the ***Photocoupler Isolation (19)*** and then transmit into the ***Local I/O (18)***.

1.5.5. Remote Digital Input/Output

Refer to the functional block diagram of the system as shown in Fig.1-6: The IMP-2 is connected with the remote I/O board (IMP-ARIO) developed by MSL of ITRI. By using the asynchronous master/slave serial communication method as well as the serial connection of the remote serial ***I/O Interface (22)***, ***Photocoupler Isolation (23)*** and ***Remote I/O Board (24)***, the system can be expanded to accommodate up to ***512 Outputs (25)*** and ***512 Inputs (26)***.

1.5.6. 8-channal Analog to Digital Converter

Refer to the functional block diagram of the system as shown in Fig. 1-6: 8 channels of ***Analog Voltage Signals (29)*** (selectable for the ranges of -5V~5V or 0V~10V) connect to the ***ADC Module (28)*** for the IMP-2 to read the voltage values (14-bit resolution) through the ***ADC Interface (27)***.

1.5.7. 8-channal Digital to Analog Converter

Refer to the functional block diagram of the system as shown in Fig. 1-6: The IMP-2 directly send commands through the ***System Control Circuit (15)*** toward the ***DAC Interface (11)***, and then converted into analog voltage command output by the ***DAC Module (12)***. The IMP-2 provides 8 channels of the analog voltage output, the output voltage range of ±10V. Each of these 8 channels of analog voltage output with an encoder feedback and a pulse output control is able to process hardware close loop control. However, when the channel is not used for hardware closed loop control, the DAC can be used separately. The voltage offset of the IMP-2 has been adjusted to be close to 0V at the factory. When the user uses the DAC function only, it is not necessary to adjust the voltage offset.

To use the hardware closed loop control mode, please refer to Section 1.5.2 for the description of the 8-axis synchronous/asynchronous close loop voltage control. In this case, due to the load circuits of the motor drive, the 0V output from the DAC may have small voltage offset from the 0V recognized by the drive. Such a small voltage offset may cause a slow drift to the motor, which is a normal occurrence. Once the close loop function is enabled, the close loop mechanism will automatically correct the drift, and the motor will be locked in this case. The magnitude of the offset can be read from the internal error counter of the IMP-2.

If the offset is too large, the user can adjust the driver's 0V offset or the variable resistor on the IMP-2. For the configuration, please refer to Section 3.2.1.

Chapter 2 Specifications

2.1. System Specifications

Item	Spec.
Dimensions	240 x 110 (mm)
Power Requirement	5V(3A) / 12V (500mA)
Frequency	System Base Frequency 100MHz External Frequency 50MHz
Central Processing Unit (CPU)	400MHz 32-bit 7 stage pipeline RISC 32KB D Cache / 32KB I Cache
Hardware Double-Precision Floating Point Unit (FPU)	100MHz 5-stage double precision FPU with 2.0 MFLOPS/MHz
Computer Peripheral Device Connector (PCI-Bus)	33MHz 32-bit 132MB/sec
DDR Controller	100MHz DDR 128MB
Ethernet Controller	10 / 100Mbps
Asynchronous Transmission Interface (UART)	115200bps
Pulse Generator Engine	8 32-bit 10MHz with DDA capability
Encoder Counter	8 32-bit 16MB Counts/s Differential Input + Digital Filtering
PID+FF Position Closed Loop Control	8 Ch 4 x 8 bits (PID & FF Gain) Parameter Register
Analog Output	8 Ch 16-bit 800k/s -10V~10V
Analog Input	8 Ch 14-bit 28.8ksps Bipolar mode: -5V~5V (Short circuit of Pin2 and Pin3 of JP1) Unipolar mode: 0V~10V (Short circuit of Pin1 and Pin2 of JP1)

Local Digital I/O (On Board)	8 OT+, 8 OT-, 8 HOME, 8 SERVO, 8 LED/SW, 1 PRDY, 1 ESTOP (Total 42 I/O)
Remote I/O Control (RIO)	Asynchronous Master/Slave Serial Transmission Protocol I/O Refresh Time: 7.2us 16 Input Points + 16 Output Points Maximun up to 512 input + 512 output
General Servo Bus	Avalible for various full digital servo driver interfaces (SSCNET III, MECHATROLINK III)

2.2. Motion Control Specifications

The IMP-2 has 8 sets of the motion control core mechanisms, each of which can be configured for closed loop control (Velocity Command) or open loop control (Pulse Command). As a result, up to M sets of closed loop control and N sets of open loop control can be used, in which M+N≦8.

In the IMP-2, there are many interrupt sources that generate interrupt signals (to be described later). Each interrupt source has a state latch value. When the interrupt occurs, the state latch value will be set to 1, and it will send an interrupt signal to the CPU through the BUS. If the CPU reads the state latch value, the value will be cleared and reset to 0. Each interrupt source can be Enabled/Disabled by the software (default: All Disabled).

2.2.1 Open Loop Control (Pulse Command)

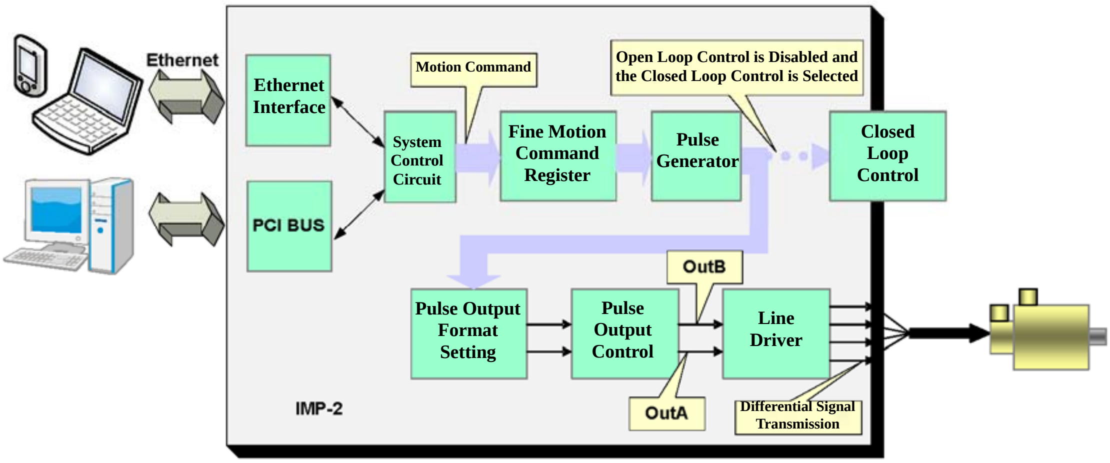


Fig. 2-1

(I) Fine Motion Command Register (FMC) FIFO: It can store 64 fine motion commands. The Pulse Generator will read commands and send out pulse for each axis after every IPO time.

- Structure: 64 commands of 32-bit FIFO (First In First Out) stock
- Command Format: Directional (1-bit), Number of Pulses (31-bit)
- Through the MCCL function, the user can know: the FIFO is full or empty, the number of remaining unexecuted commands in FIFO, and the currently processing command. For more details, please refer to the "IMP Series Motion Control Command Library Reference Manual".
- The minimum number of remaining unexecuted commands can be set. And when it equal to the the number of the remaining unexecuted commands in FIFO, the interrupt will be activated to the system.

(II) Pulse Generator:

- The Pulse Generator of each axis can be Enabled/Disabled through the software (default: Disable)
- Within each IPO Time, the maximum outputs are $0 \sim 2^{31}$ pulses.
- It can be configured to generate an interrupt to the system after each IPO Time finishes. In this case, the IMP-2 will generate an interrupt after executing each fine motion command (i.e., after each IPO Time)
- IPO Time: There are two configuration methods:
  1. Use the IDDL (IMP Series Device Driver Library, Note 1) to set the PGE Clock Divider and the PGE Clock Number to achieve this goal.

     $$\text{IPO Time} = \frac{1}{SystemClock} \times (ClockDivider + 1) \times (ClockNumber + 1)$$

  2. Use the MCCL (IMP Series Motion Control Command Library, Note 2) to directly configure the IPO Time.

  Note 1: For more details, please refer to “IMP Series Device Driver Library Reference Manual”.
  Note 2: For more details, please refer to “IMP Series Motion Control Command Library Reference Manual”.

(III) Pulse Output Format (Refer to Fig. 1-10 and Fig. 1-12)

- Pulse/Direction (Default)
- CW/CCW
- A/B phase
- None: Pulse signal output is disabled

(IV) Pulse Output Control (Refer to Fig. 2-1, the output pulses are indicated by OutA and OutB):

- OutA & OutB can be individually set as inverted output (Default: non-inverting)
- OutA & OutB can be exchanged (Default: Not exchanged)

(V) Line driver

- Use the MC3487 with 5V differential output.

2.2.2 Closed Loop Control (Velocity Command)

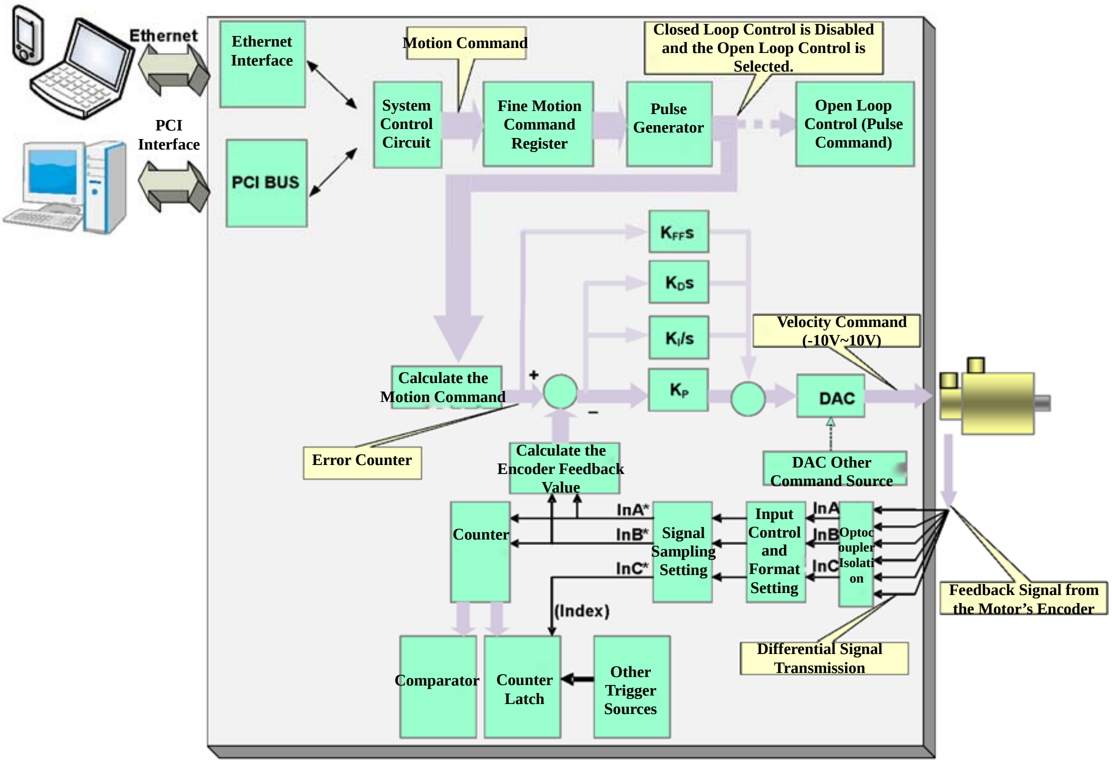


Fig. 2-2

(I) Fine Motion Command Register (Refer to Section 2.2.1 for more details)

(II) Pulse Generator (Refer to Section 2.2.1 for more details)

(III) Control Method: PID+FF

- Error Counter: 16-bit long, can be configured to generate interruption when the error counter overflows.
- K_P, K_I, K_D, and K_{FF} Control Method: It can use the MCCL function to set the proportional (K_P), integration (K_I), differential (K_D), and feedforward (K_{FF}) gain parameters in the closed loop. The range of settings is 0~127. The gain parameters can be adjusted as follows: After the driver is configured as voltage commands, using the Integrated Test Environment (ITE) provided by the installation CD-ROM to adjust the gain according to the tracking error (the tracking error is the difference between the command position and the actual position).

(IV) Velocity Command Range: Use the DAC output ±10V

2.3. Encoder Input Specifications

(I) Number of Units: 8 Channels

(II) Encoder Input Isolation

- Isolation Method: Photocoupler
- Input Frequency: Maximum 16MB counts/s

(III) Input Signals InA, InB, and InC:

- Three signals can be individually inverted (Default: non-inversed phase)
- InA and InB signal can be exchanged (Default: not exchanged)

(IV) InA, InB Input Format Setting

- A/B phase, CW/CCW, Pulse/Direction Format
- Multiplier can be set as ×0, ×1, ×2, ×4 (Default: ×4)
- None: The encoder signal input is disabled

(V) Input Signal Sampling and Digital Filter Function

- Format: Input signal must be identical in three consecutive samples to be considered as a normal signal (InA, InB, and InC)
- Sampling rate: 100MHz

(VI) Counter

- Length: 32-bit
- Enabled/Disabled (Note: For closed loop control, it must be set as Enable)
- It can be configured through the software at boot (Default: 0)
- For counting Encoder value.

(VII) Counter Latch

- It allows the user to set the Index or other triggering signal source to latch the counter for value reading. And the triggering mode can be set as single trigger or multiple triggers.
- It can be configured as Enabled/Disabled (Default: Disable) (Please refer to "IMP Series Device Driver Library User Manual")

(VIII) Index

- It can read the current state of the encoder Index signal (high/low)
- It can be configured to use the encoder's input Index to directly generate an interrupt to the system

(IX) Comparator

- When the compare counter value is equal to the predefined value in the comparator, and the Comparator Flag is set as 1 and it can also be set to generate an interrupt to the system.

(X) Encoder Interrupt Statistics

- The Index can directly generate an interrupt (8 interrupt s in total)
- When the counter value is equal to the predefined value in the comparator, it can directly generate an interrupt (8 interrupt s in total)
- The interrupt can be set as Enabled/Disabled (Default: Disable)

2.4. Digital-to-Analog converter

(I) Number of Units: 8 channels

- It can separately map the closed loop control of each axis. When the closed loop control (Velocity Command) is processed, it is necessary to use the software to direct the DAC command source to the closed loop control; when some channels of the closed loop control is not used, the DAC of the channels can be available for separate operation.
- DAC can be set as Start or Stop (Default: Stop). When DAC is set as Stop, the DAC output value remains at the value of the previous command.

(II) Resolution: 16-bit

(III) Output Voltage of the IMP-2 at Boot: 0V (If it is not 0V, please adjust the variable resistor to 0V. Please refer to Section 3.2.1)

(IV) DAC Output Interface Specifications

- External Load: Must >2KΩ
- Output Voltage: ±10V

(V) Three sources of the DAC values are listed below:

1. PCL (Closed Loop Control) Mode: It is used for closed loop control (Velocity Command).
2. Direct write buffer mode: In this mode the converted value can directly be send to the DAC to generate a voltage.
3. Trigger buffer mode: Preset a converted value in the trigger buffer. When the preset trigger signal is triggered, the preset converted value in the trigger buffer is send into the DAC to generate an output voltage. There are 8 trigger signal sources. For more details, please refer to the “IMP Series Motion Control Command Library”.

2.5. Local Digital Input/Output

(I) 25 Dedicated Inputs

- Local I/O can be controled by the CPU which is not related to other functions
- Operating Voltage: DC 24V±10%
- If the input voltage is 18V~30V (the electric potential difference between the voltage input to the COM), the internal reading is 0.
- When the input voltage is 0V~1V (the electric potential difference between the voltage input to the COM), the internal reading is 1.
- Isolation: Photocoupler
- Classification
  1. Forward limit input: Total 8 inputs, which are OT0+, OT1+, OT2+, OT3+, OT4+, OT5+, OT+6, and OT7+.
  2. Backward limit input: Total 8 inputs, which are OT0-, OT1-, OT2-, OT3-, OT4-, OT5-, OT6-, and OT7-.
  3. Home Input: 8 inputs, which are HOM0, HOM1, HOM2, HOM3, HOM4, HOM5, HOM6, and HOM7.
  4. Emergency Stop Input: 1 input, which is ESTP. When the emergency stop occurs (i.e., the emergency stop input value is 1), the hardware will disable pulse output and the DAC output value is 0V, and the built-in latch of the IMP-2 can latch the emergency stop state.

Note 1: Release the emergency stop state: Please clear the cause for the emergency stop (i.e., the user can use the MCCL function to read the emergency stop state, the reading should be 0), and then using the software to reset the IMP-2 to release the Emergency Stop state.

Note 2: For more information about the emergency stop, please refer to Section 3.2.1.

(II) 17 Dedicated Outputs

- Operating Voltage: DC 24V±10%
- Driving Method: Open collector type output
  When the internal output value of the IMP-2 is 0, it is short. If the output value is 1, it is open.
- Maximum carrying capacity for each Point: 60mA (It is not allowed to connect to 24V power without any loading.)
- Isolation: Photocoupler
- Classification
  1. Servo On/Off: 8 outputs, which are SVON0, SVON1, SVON2, SVON3, SVON4, SVON5, SVON6, and SVON7.
  2. LED On/Off: 8 outputs, which are LED0, LED1, LED2, LED3, LED4, LED5, LED6, and LED7.
  3. Position Ready: It indicates the IMP-2 is in standby state.

(III) One Internal Safety Control Outputs:

After the system is booted and before the initialization software is completed, there might be an uncertain period. To ensure that the motor will not have unexpected operation within this period, the IMP-2 is designed with a built-in dedicated safety control output that can shut down the pulse output and voltage output while system boot. After the initialization process has been completed, the MCCL will automatically enable this safety control output. The IDDL will enable the pulse output and enable the DAC output, please refer to the “IMP Series Driver Device Library Reference Manual”.

Note 1: Before enabling the safety control output, please make sure that the system is not in the emergency stop state. Otherwise, the output is invalid state. Please refer to the description for the emergency stop in the previous section.

Note 2: When the safety control output is disabled, no matters the settings in the IMP-2 are, the output pulse and output voltage are in the “Disabled” state.

2.6. Remote Digital Input/Output

(I) The IMP-2 provides RIO male plug to serially connect asynchronous remote I/O boards (IMP-ARIO). Each asynchronous remote I/O board has 16 inputs and 16 outputs. It can be expanded up to 32 modules, thus a total of 512 inputs and 512 outputs can be supported.

(II) Communication Control: Please refer to the “IMP-ARIO Hardware User Manual”

2.7. Analog-to-Digital Converter

(I) Number of Units: 8 channels

(II) Voltage Input Range:
Bipolar mode: -5V~5V
Unipolar mode: 0V~10V

(III) Resolution: 14-bit

(IV) Free Run Mode:
Among the 8 channels of ADCs, some of them can be configured for conversion and others can be disabled. Those in the enabled channels will carry out the conversion in sequence.

(V) Comparator and Comparator Interrupt

- Mask Function:
  The comparator first masks the last 0, 1, 2, or 3 bits of the voltage reading from the ADC as the masked values then compare these with the values of the comparator. The comparison result will be used to notify the CPU in interrupt.
- There are three methods can be selected to trigger the interrupt:
  1. When the masked value changes from being less than the value of the comparator to being equal to or greater than the value of the comparator
  2. When the masked value changes from being greater than or equal to the value of the comparator to being less than the value of the comparator
  3. Both of the above two conditions can trigger the interrupt.

- A value of the comparator is first defined. After the comparison, if one of the above three conditions is satisfied, it will trigger an interrupt signal to the system. Each comparator can be set to generate an interrupt signal (there will be 8 interrupt signal sources.)

2.8. Timer and Watchdog Timer

(I) Timer

- It can be set as Enabled/Disabled
- Timing Unit: System clock (10ns)
- Timer Length: 32-bit
  The setting range is 0 ~ (2^{32}-1) times of the system's clock. At the end of the timer, it can be set to generate an interrupt to the system.

(II) Watchdog Timer

- Timing Unit: The time length that can be set for the timer
- Watchdog Timer Length: 32-bit

  The setting range is 0 ~ (2^{32} – 1) times the timing unit. The user must clear the watchdog timer and set its value to zero before the watchdog timeout. When the watchdog timeout, the IMP-2 will automatically generate a reset signal (the length of the reset signal is configurable).

2.9. Reset

The Reset function can be activated not only by using the hardware switch provided on the IMP-2, but also allows the user to use software to reset individual or all the peripheral mechanisms of the IMP-2, such as the DAC, ADC, Closed Loop Control (PCL), Pulse Generator, Local I/O, Remote I/O, etc.

Chapter 3 Hardware Installation

3.1. Basic Installation

A+PC Mode:

A. Run the setup.exe in the Installation CD-ROM.

B. After the installation is completed, turn off the power, including the PC, motors, etc.

C. Connect the adapter cable (40-Pin to 68-Pin SCSI II) to the IMP-2 and then insert the IMP-2 into PCI-Bus with necessary fixation.

D. Connect the peripheral devices then connect the SCSI II 100-Pin cable and the SCSI Ⅱ 68-Pin cable to the IMP-2 and secure them with screws (for the wiring of peripheral circuits, please refer to other sections in this manual). Using the Ethernet or RS232 functions, then connect the Ethernet cable and the RS232 cable to the RJ45 connector and RS232 male header on the IMP-2.

E. Make sure that the computer, the driven motors, and I/O boards are grounded properly to ensure that they are at the same reference potential so as to avoid the system damage at start up due to different reference potential.

F. After turning on the computer, a message box ("Add new hardware") will appear on the computer screen. Follow the instruction on the screen and use the CD-ROM supplied with the board to install the software for the motion control platform.

G. The Integrated Test Environment and Sample programs delivered with the board can assist the user to test and learn activities for understanding the operation of the IMP-2.

Standalone Mode:

A. Connect external +5V, +12V and -12V power to the IMP-2.

B. Connect the adapter cable (40-Pin to 68-Pin SCSI II) to the IMP-2. Connect the peripheral devices then connect the SCSI II 100-Pin cable and the SCSI Ⅱ68-Pin cable to the IMP-2 and secure them with screws (for the wiring of peripheral circuits, please refer to other sections in this manual). Using the Ethernet or RS232 functions, then connect the Ethernet cable and the RS232 cable to the RJ45 connector and RS232 male header on the IMP-2.

C. Make sure that the IMP-2, the driven motors, and I/O modules are grounded properly to ensure that they are at the same reference potential to avoid the system damage at start up due to different reference potential.

D. For other software used in the Standalone mode, please refer to the "IMP Series Standalone Mode User Guide".

3.2. Hardware Board Layout

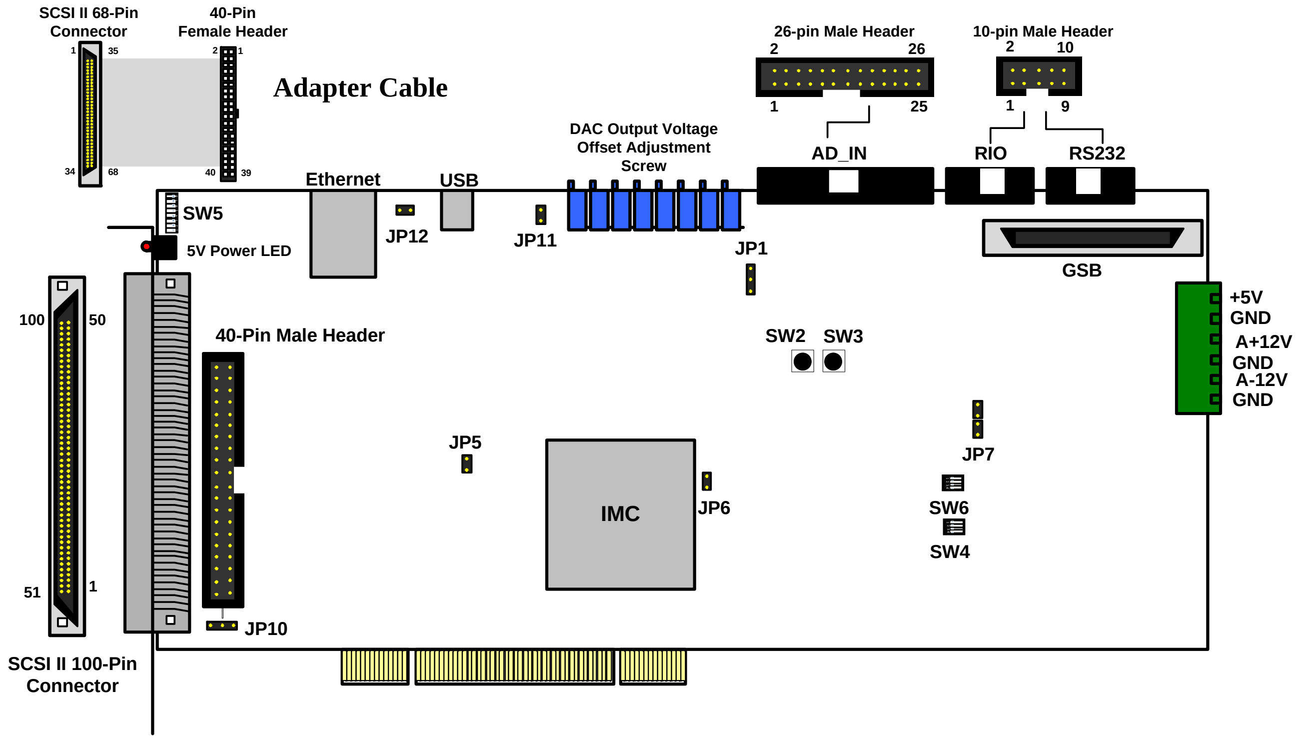


Fig. 3-1

3.2.1 Hardware Board Description

(I) The 5V power LED is on: the VCC has been supplied normally.

(II) The DAC output voltage offset adjustment screws are variable resistors: They are used for adjusting the DAC output voltage offset. In the closed loop voltage control mode, the variable resistor for each axis can be adjusted to achieve a minimum error counter value (error counter = target position — feedback position). When the DAC is used separately, the variable resistor can be adjusted for the output voltage to become 0V.

Note: From left to right: VR1 (DAC0), VR2 (DAC1), VR3 (DAC2), VR4 (DAC3), VR5 (DAC4), VR6 (DAC5), VR7 (DAC6), and VR8 (DAC7)

(III) JP1—ADC Input Mode Setting

- If the ADC input voltage range is -5V~5V, please select the Bipolar Mode (short the JP1of Pin2 and Pin3)
- If the ADC input voltage range is 0V~10V, please select the Unipolar (short the JP1of Pin1 and Pin2)
- Default setting of JP1: Bipolar Mode

(IV) JP5—Emergency Stop Mode Setting

- Short circuit the ESTOP of JP5 to disable the Emergency Stop Function (i.e., the emergency stop reading is always 0 so that the emergency stop never occur.)

- The JP5 short circuited as default. When the emergency stop circuit is connected, it is necessary to open circuit JP5 (remove the jumper) to avoid the no-action of emergency stop.
- When the ESTOP occurs, if the DAC output value is not 0V, the user can adjust the variable resistor to make the output as 0V.
- Default setting of JP5: Short circuit

(V) JP6—Boot ROM Clock Source Setting

- Open Circuit Mode: Boot ROM Clock is provided by the IMC on the IMP-2
- Short Circuit Mode: Boot ROM Clock is provided by an external oscillator or a PROM.
- Default setting of JP6: Open circuit

(VI) JP7—Boot ROM Mode Setting

- When the U40 is connected, the Boot ROM Mode must be set as the Serial Mode (Short circuit Pin1 and Pin2, and short circuit Pin3 and Pin4)
- When the U61 is connected, the Boot ROM Mode must be set as the JTAG/B-scan Mode (Short circuit Pin2 and Pin3)

(VII) JP10—LIO Mode Setting

- If the local input wiring is selected as Source Input type, the COM node of the IMP-2 must provide +24V input. In this case, it is necessary to short circuit Pin2 and Pin3 of JP10.
- If the local input wiring is selected as Sink Input type, the COM node of the IMP-2 must provide 0V input. In this case, it is necessary to short circuit Pin1 and Pin2 of JP10.
- Default setting of JP10: Source Input type
- Note: For more information about the local input wiring, please refer to Section 3.4.3.1.

(VIII) JP11—USB Master/Slave Mode Setting

- Open Circuit Mode: OTG Device Mode
- Short Circuit Mode: Host Mode
- Default setting of JP11: Open circuit

(IX) JP12—USB Device Mode Setting

- Open Circuit: B-Type
- Short Circuit: A-Type
- Default setting of JP12: B-Type

(X) SW2—System Reset (RESET)

- The user can use the hardware switch SW2 on the IMP-2 for system reset operation

(XI) SW3—Hardware Reset (PROG)

- The user can use the hardware switch SW3 on the IMP-2 for hardware reset operation

(XII) SW4—Hardware Boot Mode Setting

- The following four modes are available for selection: M[2:0]
  1. Master serial (000) (U40 is mounted)
  2. Slave serial (111) (U40 is mounted)
  3. SPI interface (001) (U61 is mounted)
  4. JTAG (101)
- Default setting of SW4: 000

(XIII) SW6—SPI Boot ROM Selection: FS[2:0]

- When U61 is mounted, the default setting of SW6: 101

3.2.2 Description of Jumper and Defualt Setting

Refer to Fig. 3-1, the function of each jumper is shown in the table below:

Jumper	Description	Default Setting
JP1	ADC Input Mode Setting	Bipolar Mode (Short circuit Pin2 and Pin3)
JP5	ESTOP Function Setting	Short Circuit
JP6	Boot ROM Clock Source Setting	Open Circuit
JP7	Boot ROM Mode Setting	Serial Mode (U40 is mounted) (Short Circuit Pin1 and Pin2, Short circuti Pin3 and Pin4)
JP10	LIO Mode Setting	Source Input type (Short Circuit Pin2 and Pin3)
JP11	USB Master/Slave Mode Setting	Open Circuit
JP12	USB Device Mode Setting	Open Circuit

As shown in Fig. 3-1, each switch is described as follows:

SW	Definition	Default Setting
SW2	System Reset (RESET)	
SW3	Hardware Reset (PROG)	
SW4	Hardware Boot Mode Setting	000
SW5	DIP Switch Reserved	
SW6	SPI Boot ROM Selection	101

3.3. Pin Assignments of Connectors

- **Pin Assignments of SCSI II 100–Pin Connector, please refer to the following table:**

SCSI II 100-Pin Connector			
Pin Assignment	**Pin**	**Pin**	**Pin Assignment**
AGND	1	51	AGND
DAC0	2	52	DAC3
DAC1	3	53	DAC4
DAC2	4	54	DAC5
+5V	5	55	COM-
COM+	6	56	COM-
COM	7	57	ESTOP
COM	8	58	PRDY
HOM0	9	59	HOM1
OT0+	10	60	OT1+
OT0-	11	61	OT1-
SVON0	12	62	SVON1
HOM2	13	63	HOM3
OT2+	14	64	OT3+
OT2-	15	65	OT3-
SVON2	16	66	SVON3
HOM4	17	67	HOM5
OT4+	18	68	OT5+
OT4-	19	69	OT5-
SVON4	20	70	SVON5
EA0+	21	71	EA1+
EA0-	22	72	EA1-
EB0+	23	73	EB1+
EB0-	24	74	EB1-
EC0+	25	75	EC1+
EC0-	26	76	EC1-
EA2+	27	77	EA3+
EA2-	28	78	EA3-
EB2+	29	79	EB3+
EB2-	30	80	EB3-
EC2+	31	81	EC3+
EC2-	32	82	EC3-
EA4+	33	83	EA5+
EA4-	34	84	EA5-
EB4+	35	85	EB5+
EB4-	36	86	EB5-
EC4+	37	87	EC5+
EC4-	38	88	EC5-
PA0+	39	89	PA1+
PA0-	40	90	PA1-
PB0+	41	91	PB1+
PB0-	42	92	PB1-
PA2+	43	93	PA3+
PA2-	44	94	PA3-
PB2+	45	95	PB3+
PB2-	46	96	PB3-
PA4+	47	97	PA5+
PA4-	48	98	PA5-
PB4+	49	99	PB5+
PB4-	50	100	PB5-

- **Pin Assignment of 40-Pin Male Header, please refer to the following table**

40-Pin Male Header			
Pin Assignment	**Pin**	**Pin**	**Pin Assignment**
AGND	1	2	AGND
DAC6	3	4	DAC7
HOM6	5	6	HOM7
OT6+	7	8	OT7+
OT6-	9	10	OT7-
SVON6	11	12	SVON7
EA6+	13	14	EA7+
EA6-	15	16	EA7-
EB6+	17	18	EB7+
EB6-	19	20	EB7-
EC6+	21	22	EC7+
EC6-	23	24	EC7-
PA6+	25	26	PA7+
PA6-	27	28	PA7-
PB6+	29	30	PB7+
PB6-	31	32	PB7-
NC	33	34	NC
NC	35	36	NC
NC	37	38	NC
GND	39	40	GND

- **Pin Assignment of Adapter Cable (SCSI Ⅱ 68-Pin Connector), please refer to the following table**

SCSI II 68-Pin Connector			
Pin Assignment	**Pin**	**Pin**	**Pin Assignment**
AGND	1	35	AGND
DAC6	2	36	DAC7
HOM6	3	37	HOM7
OT6+	4	38	OT7+
OT6-	5	39	OT7-
SVON6	6	40	SVON7
EA6+	7	41	EA7+
EA6-	8	42	EA7-
EB6+	9	43	EB7+
EB6-	10	44	EB7-
EC6+	11	45	EC7+
EC6-	12	46	EC7-
PA6+	13	47	PA7+
PA6-	14	48	PA7-
PB6+	15	49	PB7+
PB6-	16	50	PB7-
NC	17	51	NC
NC	18	52	NC
NC	19	53	NC
GND	20	54	GND
NC	21	55	NC
NC	22	56	NC
NC	23	57	NC
NC	24	58	NC
NC	25	59	NC
NC	26	60	NC
NC	27	61	NC
NC	28	62	NC
NC	29	63	NC

NC	30	64	NC
NC	31	65	NC
NC	32	66	NC
NC	33	67	NC
NC	34	68	NC

- **Pin Assignment of SCSI II 100-Pin Connector & SCSI II 68-Pin Connector - PGE Signal Output:**

Name	Description	Reference
PAn+ & PAn- (n=0~7)	The Phase A output signals from the n^{th} axis PGE, through the line driver in the differential format	GND
PBn+ & PBn- (n=0~7)	The Phase B output signals from the n^{th} axis PGE, through the line driver in the differential format	GND

- **Pin Assignment of SCSI II 100-Pin Connector & SCSI II 68-Pin Connector - Encoder Signal Input:**

Name	Description	Refernce
EAn+ & EAn- (n=0~7)	The Phase A differential input signals of the n^{th} axis Encoder Counter	GND
EBn+ & EBn- (n=0~7)	The Phase B differential input signals of the n^{th} axis Encoder Counter	GND
ECn+ & ECn- (n=0~7)	The Phase C differential input signals of the nt^{h} axis Encoder Counter	GND

- **Pin Assignment of SCSI II 100-Pin Connector & SCSI II 68-Pin Connector - Local I/O:**

Name	Description	Reference
OTn+ (n=0~7)	Positive-travel limit input of the nth axis	COM
OTn- (n=0~7)	Negative-travel limit input of the nth axis	COM
HOMn (n=0~7)	Home input of the nth axis	COM
ESTOP	Emergency Stop Input	COM
SVONn (n=0~7)	The Servo On output of the n^{th} axis	COM-
PRDY	Position ready output	COM-
COM+	Power terminal (+) of Local Digital Output	

COM-	Power terminal (-) of Local Digital Output	
COM	Common terminal of Local Digital Input	

- **Pin Assignment of SCSI II 100-Pin Connector & SCSI II 68-Pin Connector - D/A Converter Output and Other:**

Name	Description	Reference
DACn(n=0~7)	The DAC voltage output of the n^{th} axis or the speed command of the n^{th} axis	AGND
+5V	DC +5V output (Max. Current: 500mA)	GND
AGND	Analog GND	

- **Pin Assignment of RIO Connector:**

  Refer to the following figure

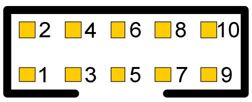


Fig. 3-2 10-Pin Male Header

Name	Pin	Description	Reference
Tx+ & Tx-	9 and 4	Serial data sent by the Master (IMP-2) to the Slave (IMP-ARIO) in differential format	GND
Rx+ & Rx-	8 and 3	Serial data sent by the Slave (IMP-ARIO) to the Master (IMP-2) in differential format	GND
GND	5 and 10	GND	
N / A	1, 2, 6, 7	For expansion	

- **Pin Assignment of ADC Connector**

  Refer to the following figure

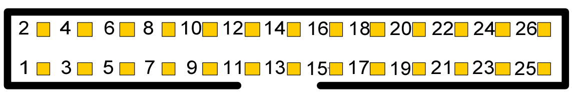


Fig. 3-3 26-Pin Male Header

Name	Pin	Description	Reference
ADC0+	1	Positive terminals of the 0^{th} ADC analog differential input signal	AGND

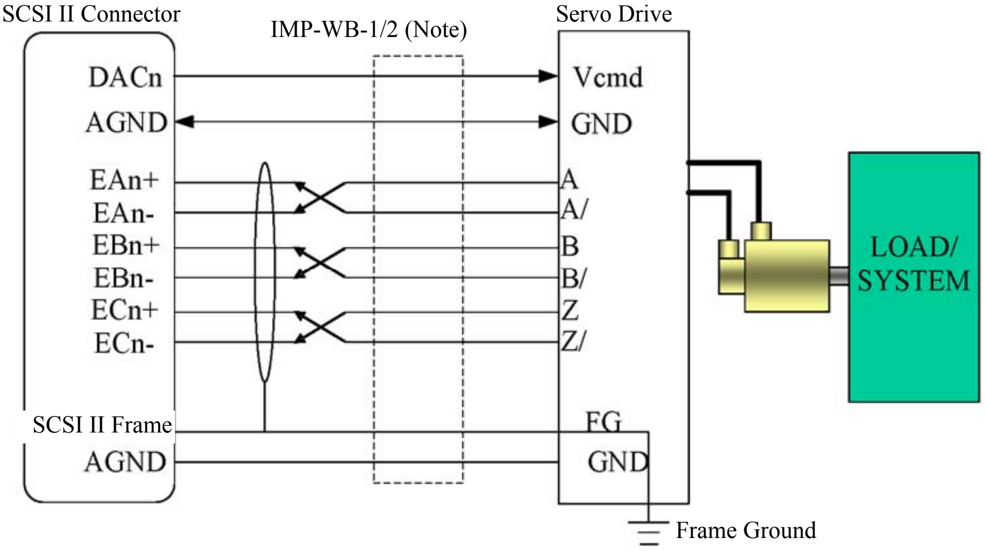
ADC0-	3	Negative terminals of the 0^{th} ADC analog differential input signal	AGND
ADC1+	5	Positive terminals of the 1^{th} ADC analog differential input signal	AGND
ADC1-	7	Negative terminals of the 1^{th} ADC analog differential input signal	AGND
ADC2+	9	Positive terminals of the 2^{th} ADC analog differential input signal	AGND
ADC2-	11	Negative terminals of the 2^{th} ADC analog differential input signal	AGND
ADC3+	13	Positive terminals of the 3^{th} ADC analog differential input signal	AGND
ADC3-	15	Negative terminals of the 3^{th} ADC analog differential input signal	AGND
ADC4+	2	Positive terminals of the 4^{th} ADC analog differential input signal	AGND
ADC4-	4	Negative terminals of the 4^{th} ADC analog differential input signal	AGND
ADC5+	6	Positive terminals of the 5^{th} ADC analog differential input signal	AGND
ADC5-	8	Negative terminals of the 5^{th} ADC analog differential input signal	AGND
ADC6+	10	Positive terminals of the 6^{th} ADC analog differential input signal	AGND
ADC6-	12	Negative terminals of the 6^{th} ADC analog differential input signal	AGND
ADC7+	14	Positive terminals of the 7^{th} ADC analog differential input signal	AGND
ADC7-	16	Negative terminals of the 7^{th} ADC analog differential input signal	AGND
AGND	17~26	ANALOG GND is the common GND for VCC_OUT, DAC OUTPUT and ADC. It is connected with DGND (DIGITAL GND).	

For other pin's assignments, please refer to the Board Layout shown in Fig. 3-1

3.4. Wiring

3.4.1. 8-Axis Synchronous/Asynchronous Closed Loop Control

The connection between the IMP-2 and the servo motor drive (velocity mode) is shown in the following figure below.



Note: This figure is an example for any axis of the IMP-2. Use the same diagram for other axis (where n=0~7)

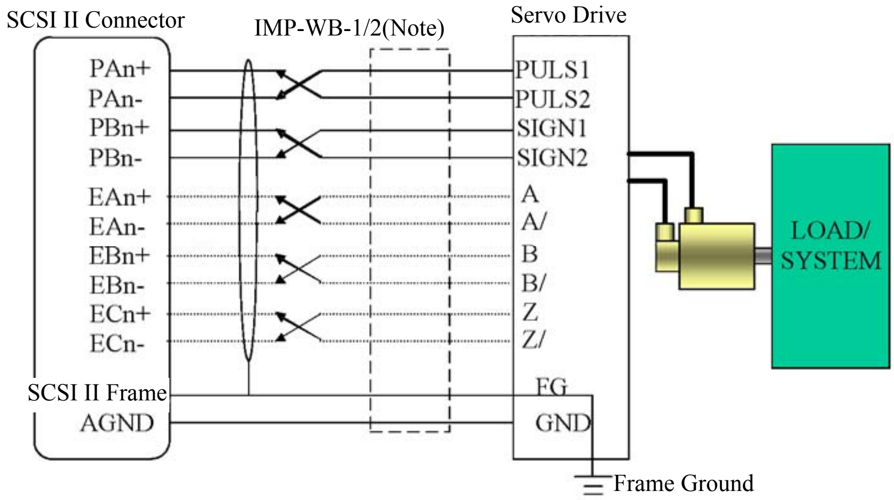
Fig. 3-4

- DACn is the velocity command (voltage command format) output of the nth axis closed loop control mechanism. It should be connected to the Vcmd (velocity Commad) input of the nth axis servo driver while the common ground (AGND) of DACn should be connected with the common ground (GND) for the Vcmd of the same axis.
- The motor encoder signal of the servo driver (A/B/Z signal) must be connected to the IMP-2 (as shown in Fig. 3-4) in the differential format. It is recommended to use twisted-pair cable for the three sets of signals A and A/, B and B/, Z and Z/ to reduce the common mode noise. In addition, use the shielding mesh to isolate the three pairs of wires from the external environment to reduce the external transmission interference.
- Connect one side of the shielding mesh to the external cases of the SCSI II 100-Pin and SCSI II 68-Pin connectors of the IMP-2 and connect the other side to the FG (Frame Ground) of the servo driver. Make sure that the PC and the servo driver are connected to the frame ground (Note: The external case of the SCSI II 100-Pin connector is connected to the frame of the PC because the frame of the PC is usually connected to the frame ground).
- Important---There should be a ground wire for connecting the GND of the servo drive to the AGND of the IMP-2 (This is very important because fatal damage may occur).

Note: Available adapters:
IMP-WB-1: Universal adapter.
IMP-WB-2: Dedicated adapter for Panasonic (Panasonic Minas A5). This adapter is also workable with using specific adapter cable for specific manufacturers (Mitsubishi MR-J3, Delta ASDA-A2, Yaskawa Σ-V).

3.4.2. 8-Axis Synchronous/Asynchronous Open Loop Control

The following is the system connection diagram for the connection between the IMP-2 and Servo Motor/Stepper Motor (Pulse mode)



Note: This figure is an example for any axis of the IMP-2. Use the same diagram for other axis (where n=0~7)

Fig. 3-5

- PAn+, PAn-, PBn+, and PBn- are the pulse command output signals of the nth axis open loop control mechanism. They are connected to the PULS1, PULS2, SIGN1, and SIGN2 of the nth axis servo drive, respectively, as shown in the figure (please refer to the servo drive operation manual).
- It is recommended to use twisted-pair cable to reduce the common mode noise. In addition, use the shielding mesh to isolate the signal of cables from the external environment to reduce the external transmission interference.
- Connect one side of the shielding mesh to the external cases of the SCSI II 100-Pin and SCSI II 68-Pin connectors of the IMP-2 and connect the other side to the FG (Frame Ground) of the servo driver. Make sure that the PC and the servo driver are connected to the frame ground (Note: The external case of the SCSI II 100-Pin connector is connected to the frame of the PC because the frame of the PC is usually connected to the frame ground).
- Important---There should be a ground wire for connecting the GND of the servo drive to the AGND of the IMP-2 (This is very important because fatal damage may occur).

Note 1: Available adapters:

IMP-WB-1: Universal adapter.

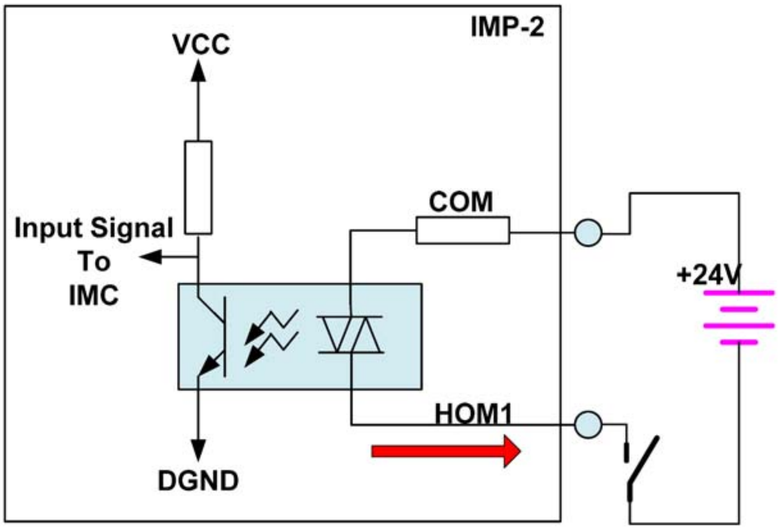
IMP-WB-2: Dedicated adapter for Panasonic (Panasonic Minas A5). This adapter is also workable with using specific adapter cable for specific manufacturers (Mitsubishi MR-J3, Delta ASDA-A2, Yaskawa Σ-V).

Note 2: The Panasonic A5 series servo drive representation.

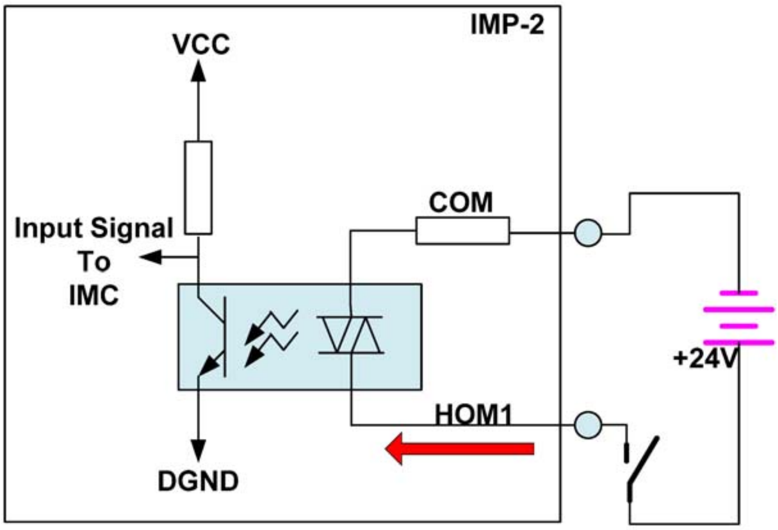
Note 3: When the Home returning mode is used, the encoder feedback signal of the servo drive must be connected to the IMP-2.

3.4.3. Local Input/Output Wiring

3.4.3.1. Local Input Wiring



Wiring 1: Source Input Type



Wiring 2: Sink Input Type

Fig. 3-6

- The HOM1 input wiring is used in the above figure as an example. Use the same diagrams for other input in a similar manner.
- There are two input types: Source Input Type and Sink Input Type.
- When the switch is short, the reading of HOM1 is 0.
- When the switch is open, the reading of HOM1 is 1.
- +24VDC power should be provide.
- Note: When a mechanical switch is used, please be aware of the bouncing effect due to tripping.

3.4.3.2. Local Output Wiring

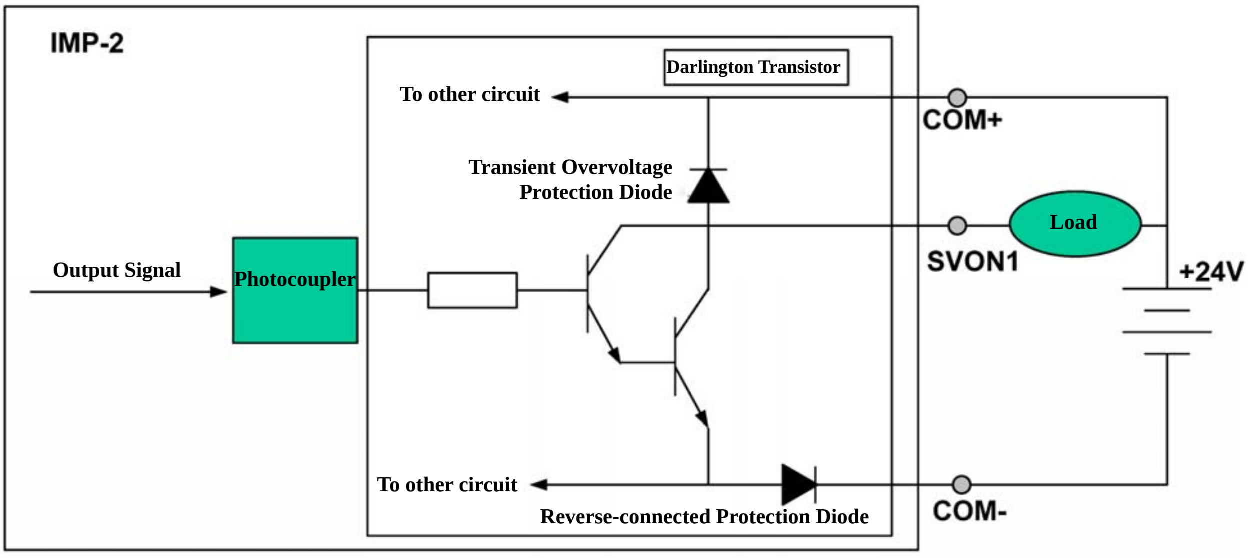


Fig. 3-7

- The SVON1 output wiring is used in the above figure as an example, which is a Sink Output Type. Use the same diagram for other output in a similar manner.
- When the output signal is 0, the transistor (Darlington driving stage) is short and the load is activated.
- **Danger**: The maximum driving capability of each output is 60mA. If there is no load, please do not connect the 24V power directly to the output.
- When the load is a RELAY, because that the Darlington transistors have the transient over-voltage protection diode, there is no need to connect external protection diode to absorb the surge noise.

3.4.4. Remote Input/Output (RIO) Wiring

The connection between the IMP-2 and IMP-ARIO are shown in Fig. 3-8. One terminal of the cable on the ***serial port PCI bracket*** is connected with a 10-Pin female header which matches the 10-Pin male header on the ***IMP-2.*** The other terminal of the cable on the ***serial port PCI bracket*** is the DB9 female socket which matches the DB9 male plug of the ***cable***. The other terminal of the DB9 male plug of the ***cable*** is connected to the DB9 female socket of the ***IMP-ARIO*** module. For more detailed descriptions, please refer to Fig. 3-9 and Fig. 3-10.

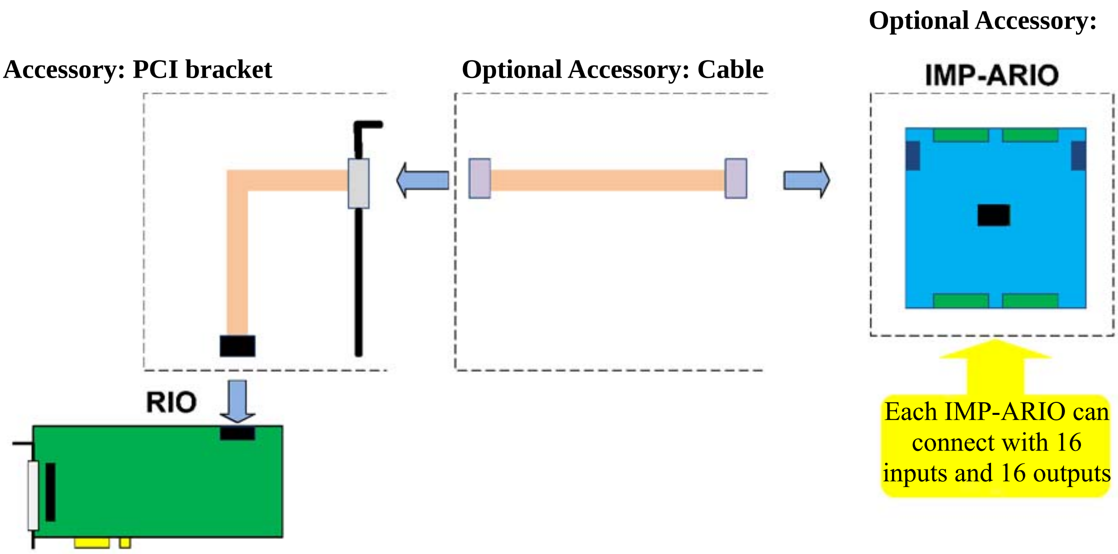


Fig. 3-8 Diagram of the connection between the IMP-2 and IMP-ARIO

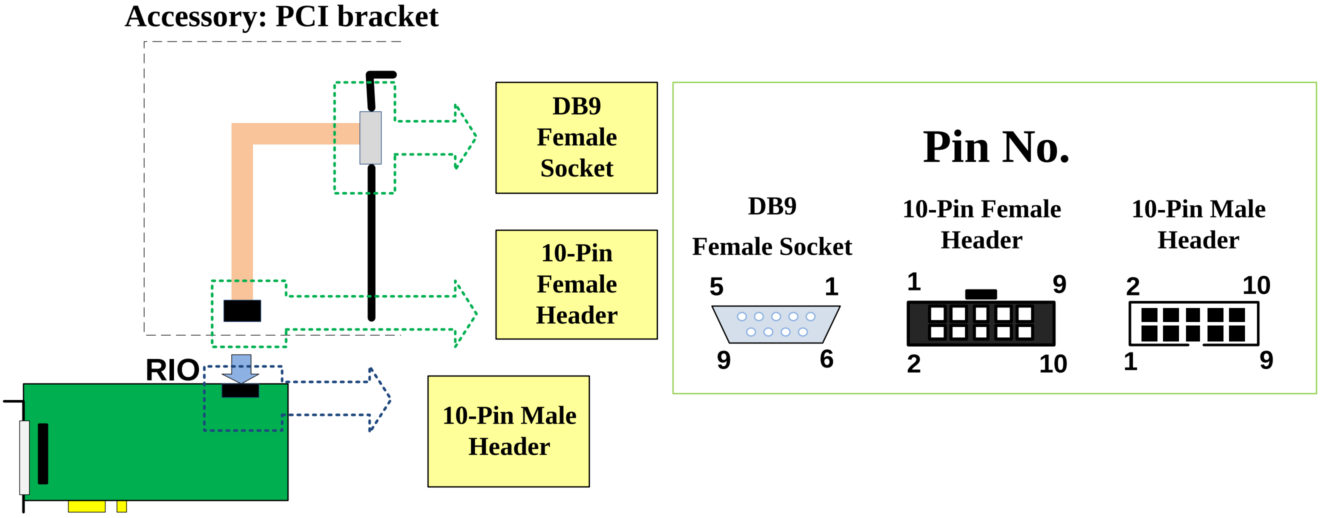


Fig. 3-9 Description of the PCI bracket

Internal Connection of the Ribbon Cable on the PCI bracket	
10-Pin Female Header	**DB9 Female Socket**
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	Not Connected

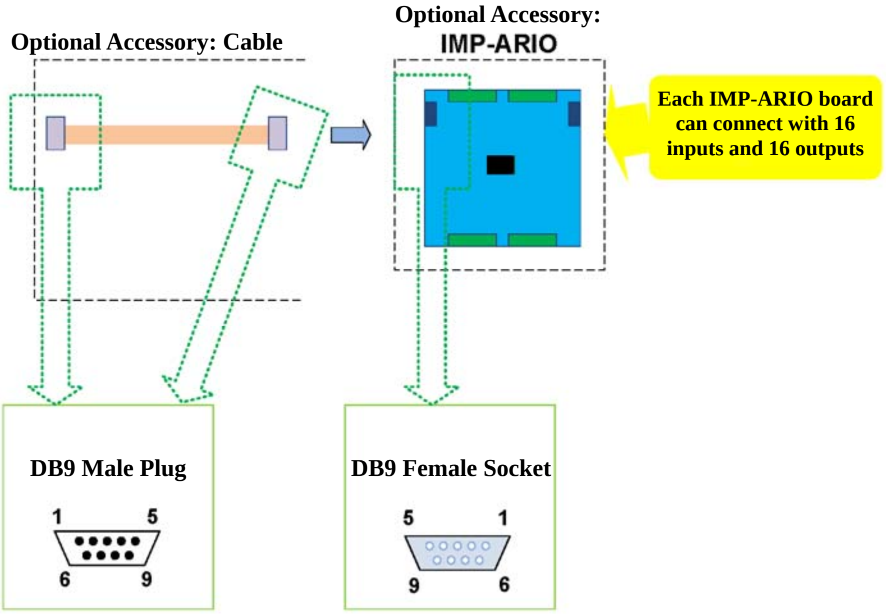


Fig.3-10 Description of the cable and the connector on the IMP-ARIO

Internal Connection of the Ribbon Cable	
DB9 Male Plug	**DB9 Male Plug**
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9

Pin Assignment of IMP-ARIO DB9 Female Socket	
1	For expansion
2	For expansion
3	Rx-
4	Tx-
5	GND
6	For expansion
7	For expansion
8	Rx+
9	Tx+

3.4.5. ADC Wiring and Description

One terminal of the ribbon cable on the serial port PCI bracket is a 26-Pin female header for connecting to the 26-Pin male header on the IMP-2. The other terminal is the DB25 female socket to pick up the ADC signal while connecting to external port.

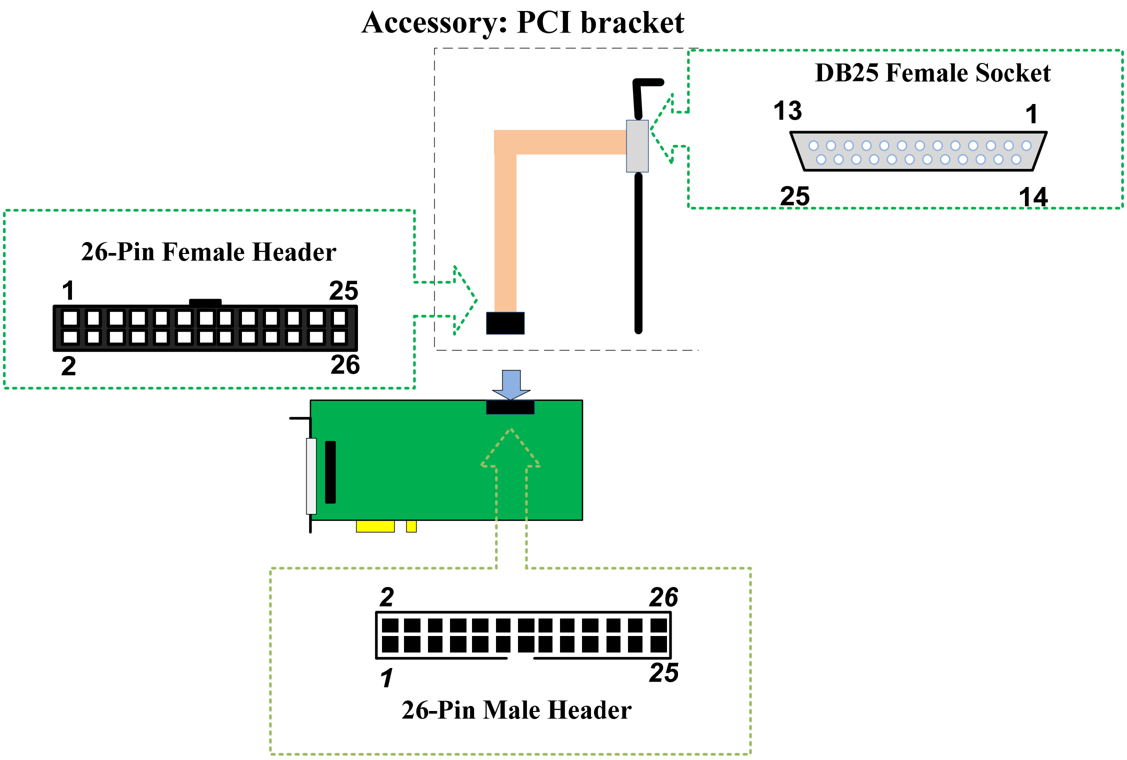


Fig. 3-11 Descriptions of the ADC connector on the IMP-2

Internal Connection of the Ribbon Cable on the serial port PCI bracket			
26-Pin Female Header (Pin1~Pin13)	DB25 Female Socket	26-Pin Female Header (Pin14~Pin26)	DB25 Female Socket
1	1	14	20
2	14	15	8
3	2	16	21
4	15	17	9
5	3	18	22
6	16	19	10
7	4	20	23
8	17	21	11
9	5	22	24
10	18	23	12
11	6	24	25
12	19	25	13
13	7	26	Not Connected

Pin Assignment of ADC 26-Pin Male Header			
1	ADC0+	2	ADC4+
3	ADC0-	4	ADC4-
5	ADC1+	6	ADC5+
7	ADC1-	8	ADC5-
9	ADC2+	10	ADC6+
11	ADC2	12	ADC6-
13	ADC3+	14	ADC7+
15	ADC3-	16	ADC7-
17~26	AGND		

Refer to the following table for the section of the wiring method:

DUT Device Under Test	Description	Connection Method
Single Ended Input	DUTs have the same ground	Connect the voltage to the ADCn+,while the ADCn- is connected to AGND (n=0~7)
Differential Input	DUTs have the same ground	Connect the input differential signals to ADCn+ and ADCn-(n=0~7) respectively.

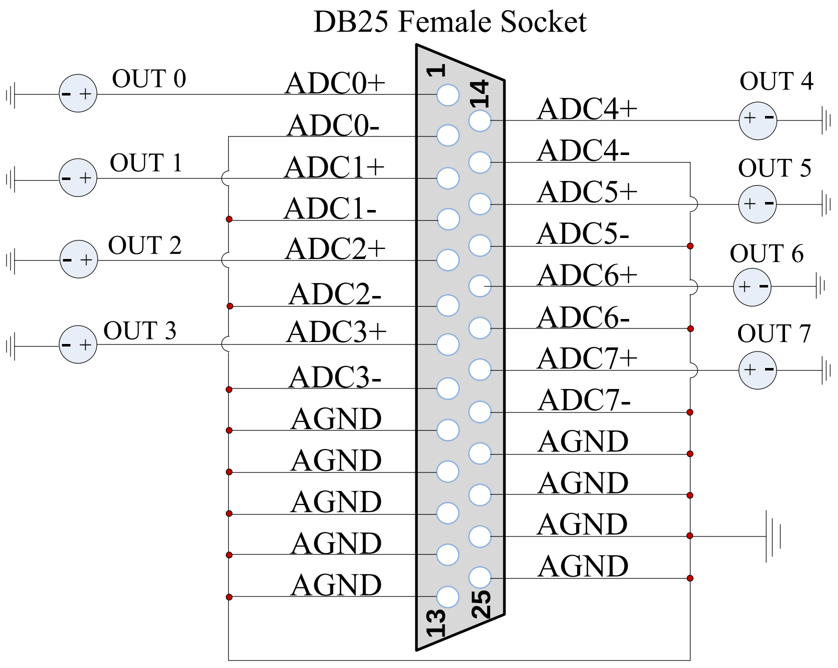


Fig.3-12 Wiring of Single Ended Input

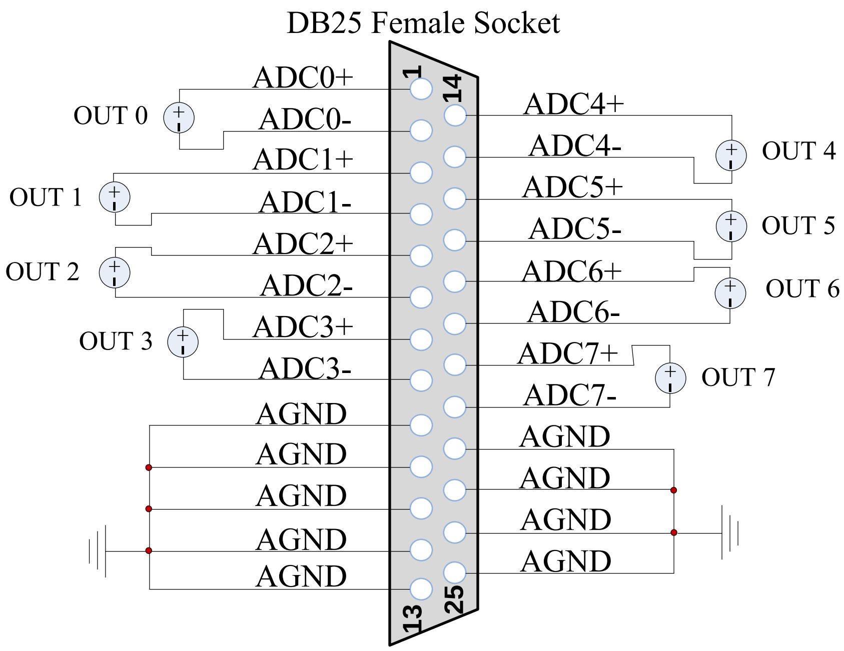


Fig.3-13 Wiring of the Differential Input

Revision History

Date	Rev.	Contents of Revision
2013/07/08	V.1.1.0	Correction of version contents and update of drawings
2016/05/04	V.1.2.0	Correction of version contents and update of drawings